**Implementation of low power cache memory using 4T SRAM**

**Motivation:**

Power and area reduction in SoC based embedded systems, are one of the important design specifications of VLSI design. This project deals with the reduction in power and area consumed by memory in SoC with acceptable trade off of stability and performance.

SoCs integrate multiple functions on a single silicon die. As process geometries have scaled, designs which use more and more of the additional silicon real estate available on chips to integrate embedded memories evolved. These embedded memories allow for significantly better system performance and lower power compared to a solution where off-chip memories are used. Most current designs have over 50% of their area used by embedded memories and these memories account for 50-70% of the total SoC power dissipation. Clearly, any attempt to reduce SoC power is incomplete if it does not attempt to reduce the power consumed by the embedded memories in the design.

Most memories embedded in SoCs are static RAMs. In order to achieve lower power consumption and less area for SRAMs, 4T SRAM structure can be used. The 4T SRAM suffers low static noise margin (SNM) and other stability issues compared with commonly used 6T SRAM. can be used to improve the SNM and stability of 4T SRAM. In this project these techniques are implemented on a 4T SRAM cache and results are verified.

**Objective:**

The objective of this project is to design a cache memory using 4T SRAM and compare it with conventional 6T SRAM cache for parameters like power, area, stability and speed of operation. Then implement different power reduction techniques on designed 4T SRAM cache to get an optimized design with low power and less area.

**References:**

1. “A low power and high density cache memory on novel SRAM cell” by ArashAziziMazreah, Mohammad Noorollahi Romani, Mohammad TaghiManzuri and Ali Mehrparvar.

**Publication:** IEICE Electronics Express, Vol.6, No. 15,1084-1090

**Objective:** This paper presents a novel CMOS four transistor (4T) SRAM cell for very high density and low power cache applications. A design for 4T SRAM was proposed and compared with conventional 6T SRAM.

**Specifications:** supply voltage is 1.2V and fabricated in a 65-nm technology.

**Tool:** HSPICE simulation tool.

**Result:** The new cell size is 20% smaller than a conventional 6T cell using same design rules. Dynamic and static power consumption of new cell is 40% and 20% smaller than 6T SRAM cell.

1. “A Low-Power Embedded SRAM for Wireless Applications” by Stefan Cosemans, Wim Dehaene and Francky Catthoor.

**publication:** IEEE journal of solid state circuits, VOL. 42, NO. 7, JULY 2007

**objective:** This paper introduces a novel ultra-low-power SRAM. A large power reduction is obtained by the use of four new techniques that allow for a wider and better trade-off between area, delay and active and passive energy consumption for low-power embedded SRAMs. The implemented design techniques consist of a more efficient memory data bus, the exploitation of the dynamic read stability of SRAM cells, a new low-swing write technique and a distributed decoder. The feasibility of proposed techniques is confirmed by implementing them on a 5T SRAM array.

**Specifications:** An 8-KB 5T SRAM was fabricated in a 0.18-µm technology. Supply voltage is 1.6V.

**Result:** The measurement results confirm the feasibility and the usefulness of the proposed techniques. A reduction of active power consumption with a factor of 2 is reported as compared to the current state of the art. The results are generalized towards a 32-KB SRAM.

1. “Low power SRAM design using hierarchical divided bit-line approach” by Ashish Karandikar

**Objective:** this paper presents a novel hierarchial divided bit-line approach for reducing active power in SRAMs by reducing bit-line capacitance. Two or more 6T SRAM cells are combined together to divide the bit-line into several sub bit lines. These sub bit-lines are again combined to form two or more levels of hierarchy. This division of bit-line into hierarchical sub bit-line results in reduction of bit-line capacitance, which reduces active power and access time. Optimum values for number of levels of hierarchy and number of blocks combined at each level have been derived. Experimental results show that the observd parameters and estimated ones follow the same trend. It is shown that the reduction in it-line capacitance reduces active power consumption by 50%-60% and the access time by about 20% at the expense of approximately 5% increase in the number of transistors. This approach is further extended by incorporating the controlled voltage swing on bit-lines. This extension reduces the power consumption by another 20%-30%.

**Introduction:** designing a low power system not only reduces weight and size of batteries for portable system but also helps in reducing the ever important packaging costs of integrated circuit. To this end, the design of low power digital system is becoming increasingly important with memories accounting for the largest share of power consumption in the processors. An emphasis has been placed on the design of low power memories.

Active power is a major component of the total memory power. This paper first describes a novel divided bit-line approach for reducing the active power by reducing the bit-line capacitance and ten extends it to a hierarchical divided bit-line approach. It is shown that by reducing this capacitance, not only power reduction is achieved but access time is reduced as well. While hierarchical word decoding has been used to reduce power consumption by reducing the number of columns activated during a read operation, this paper is the divided bit-line concept. Another advantage of this approach is the sub bit-line, SRAM cells become more stable, as they are guarded from the noise on bit-line through pass transistors.